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 [NPTEL \(https://swayam.gov.in/explorer?ncCode=NPTEL\)](https://swayam.gov.in/explorer?ncCode=NPTEL) » Microprocessors And Microcontrollers (course)


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Course
outline

About
NPTEL ()

How does an
NPTEL
online
course
work? ()

Week 0 : ()

Week 1 ()

Week 2 ()

Week 3 ()

Week 4 ()

Week 5 ()

Week 9 : Assignment 9

The due date for submitting this assignment has passed.

Due on 2025-03-26, 23:59 IST.

As per our records you have not submitted this assignment.

1) **ARM10TDMI is a** **1 point**

- a) 3-stage pipeline processor
- b) 5-stage pipeline processor
- c) 6-stage pipeline processor
- d) 8-stage pipeline processor

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:

c.

2) **1 point**

Week 6 ()**Week 7 ()****Week 8 ()****Week 9 ()**

Lecture 42 :
ARM (Contd.)
(unit?
unit=91&lesso
n=92)

Lecture 43 :
ARM(Contd.)
(unit?
unit=91&lesso
n=93)

Lecture 44 :
ARM (Contd.)
(unit?
unit=91&lesso
n=94)

Lecture 45 :
ARM (Contd.)
(unit?
unit=91&lesso
n=95)

Lecture 46 :
ARM (Contd.)
(unit?
unit=91&lesso
n=96)

Lecture
Material (unit?
unit=91&lesso
n=97)

**Quiz: Week 9
: Assignment
9
(assessment?
name=215)**

Feedback
Form (unit?
unit=91&lesso
n=163)

Week 09 :
Assignment
Solution (unit?)

In an ARM-based processor with a multi-stage pipeline, which of the following is true regarding bus architecture?

- a) Both instruction and data buses use the same width
- b) The instruction bus is narrower than the data bus for performance optimization
- c) The data bus is narrower than the instruction bus for memory efficiency
- d) The instruction and data buses have dynamically adjustable widths

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

b.

3)

All ARM instructions are

- a) 8-bit long
- b) 16-bit long
- c) 32-bit long
- d) 64-bit long

1 point

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

c.

4)

ARM instruction set supports

- a) Single load/store instructions only
- b) Multiple load/store instruction that allow to load/store upto 4 registers at once
- c) Multiple load/store instruction that allow to load/store upto 8 registers at once
- d) Multiple load/store instruction that allow to load/store upto 16 registers at once

1 point

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

d.

unit=91&lesson=201)

Week 10 ()

Week 11 ()

Week 12 ()

Download Videos ()

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5)

1 point

When a procedure call is made, the return address is automatically placed into

- a) Program Counter (R15)
- b) Link Register (R14)
- c) Stack Pointer (R15)
- d) Stack Pointer (R13)

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:

b.

6)

1 point

When the processor encounters a software interrupt instruction, ARM processor enters in

- a) Fast interrupt processing mode (FIQ)
- b) Normal interrupt processing mode (IRQ)
- c) Supervisor mode (SVC)
- d) Abort mode

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:

c.

7)

1 point

CPSR cannot be modified in which of the following mode?

- a) Fast interrupt processing mode (FIQ)
- b) Normal interrupt processing mode (IRQ)
- c) User mode
- d) Supervisor mode (SVC)

- a.
- b.

- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

c.

- 8) **On reset, ARM inserts in which of the following mode?** **1 point**
- a) Fast interrupt processing mode (FIQ)
 - b) Normal interrupt processing mode (IRQ)
 - c) Supervisor mode (SVC)
 - d) User mode

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

c.

- 9) **Which of the following ARM instructions is same as multiplying the contents of r0 by nine and storing the product in r7?** **1 point**
- a) ADD r0, r7, r7, LSL #3
 - b) ADD r0, r7, r0, LSL #3
 - c) ADD r7, r7, r0, LSL #3
 - d) ADD r7, r0, r0, LSL #3

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

d.

- 10) **1 point**

Which of the following instructions corresponds to a Multiply Accumulate instruction in ARM architecture?

- a) MUL
- b) UMULL
- c) SMULL
- d) SMLAL

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

d.

11)

1 point

Which of the following instructions corresponds to loading a signed half word in ARM architecture?

- a) LDR
- b) LDRS
- c) LDRSH
- d) LDRH

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

c.

12)

Which register is not allowed in ARM multiplication instructions?

1 point

- a) R0
- b) R1
- c) R14
- d) R15

- a.
- b.
- c.

d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

d.

13)

1 point

Which algorithm used for multiplication operations in ARM processor?

- a) Braun array signed multiplier
- b) Booth's algorithm for multiplication
- c) Baugh wooley multiplier
- d) Vedic multiplier

a.

b.

c.

d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

b.

14)

1 point

For the instruction below, which of the following statement is TRUE?

EQADD R0, R1, R2

- a) $R0 = R1 + R2$ Only if parity flag is set
- b) $R0 = R1 + R2$ Only if zero flag is set
- c) $R0 = R1 + R2$ Only if carry flag is set
- d) $R0 = R1 + R2$ Only if zero flag is reset

a.

b.

c.

d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

b.

15)

1 point

Which part of an ARM instruction contains one of the 16 condition codes?

- a) Bit 24 to bit 21
- b) Bit 31 to bit 28
- c) Bit 19 to bit 16
- d) Bit 15 to bit 12

- a.
- b.
- c.
- d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

b.